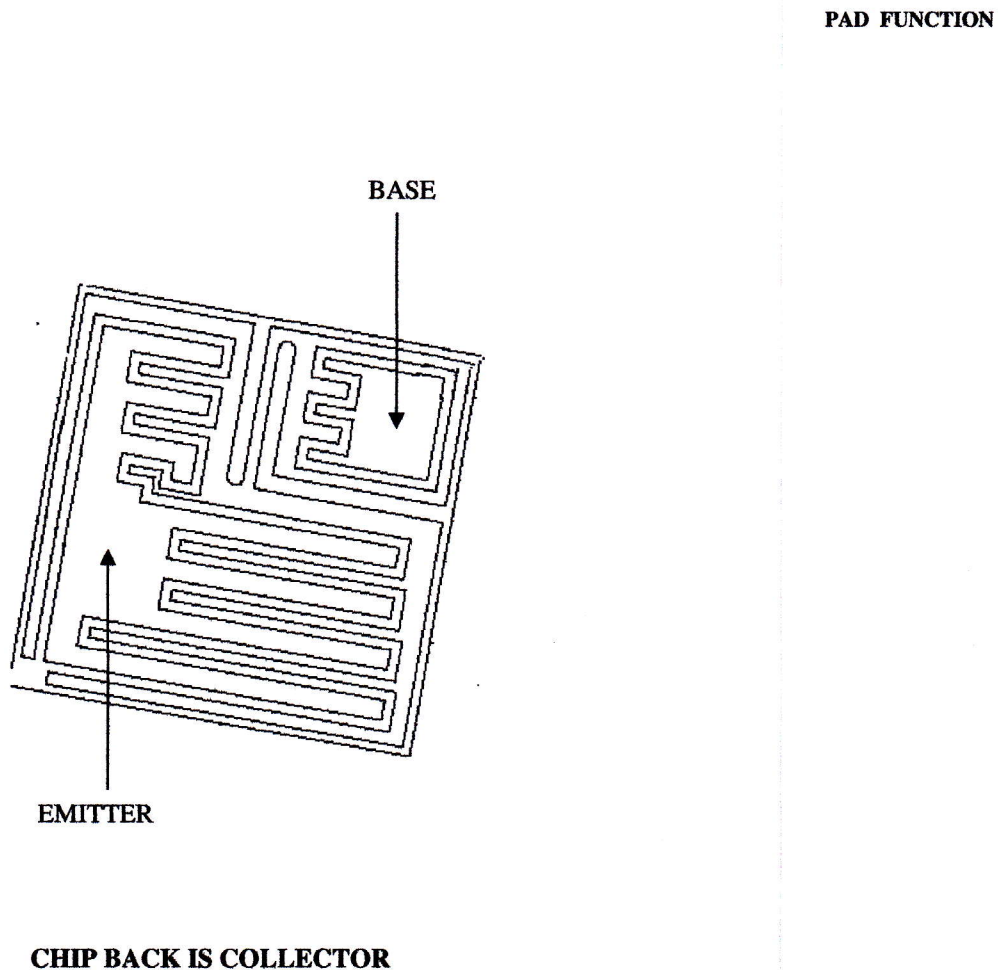




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The information for this layout is believed to be correct at the time of issue.
 Please verify your requirements prior to commencement of any assembly process, as no liability for omission or error can be accepted.
 Chip back potential is the level at which bulk silicon is maintained either by bond pad connection or in some cases the potential to which the chip back must be connected if stated above.

Note: 1 mil = 0.001 inch

<u>APPROVED</u> G Bibby DATE: 10 Jan 2005	2N6052 ON SEMICONDUCTOR	<u>DIE INFORMATION</u> DIMENSIONS (Mils): 200 x 200 x 14 BOND PADS (Mils): MASK. REF: GEOMETRY: BACK POTENTIAL: COLLECTOR
DG 10.1.2 Rev B, 7/19/02		<u>METALLISATION</u> TOP: Al BACK: TiNiAg